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SYSTEM AND METHOD FOR TRANSMISSION AND RECEPTION

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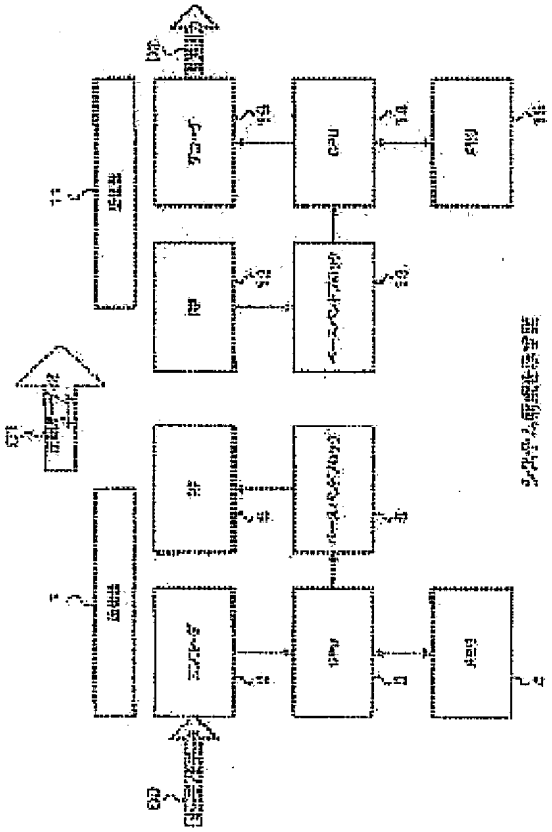
Abstract of **JP 2003087185 (A)**

PROBLEM TO BE SOLVED: To provide a system and method for transmission and reception by which average power consumption is reduced by periodically controlling the power utilizing the feature of real-time transfer. SOLUTION: The transmission side 1 of the transmission and reception system has an encoder part 2 for switching an encoder according to an input signal, a CPU 3 which is shifted to a sleep state by suspending transmission operation based on a sleep period by changeably setting the sleep period in which the sleep state is generated by suspending transmission operation according to an encoding signal, and a base band block part 5 and an RF part 6 for inserting the sleep period to a packet and transmitting it. A receiving side 11 has an RF part 12 and a base band block part 13 for receiving the packet, a decoder part 16 for switching a decoder according to the packet and a CPU 14 for extracting the sleep period from the packet and suspending receiving operation based on the sleep period to be shifted to the sleep state.



CLAIMS

[Claim(s)]

[Claim 1]A transmission and reception system which it transmits to an input signal by performing sending-signal processing from a sending set characterized by comprising the following in a network, and performs and outputs a reception signal processing to an input signal received in a receiving set in the above-mentioned network.

An encode means which changes an encoder according to the above-mentioned input signal.

A sleep period setting-out means to set a sleep period which stops a send action according to an encode signal from the above-mentioned encode means, and is made into sleeping to an enabled change.

A memory measure which memorizes the above-mentioned sleep period.

A control means which stops a send action based on the above-mentioned sleep period, and shifts to sleeping.

A transmitting means which inserts in a packet the above-mentioned sleep period memorized by the above-mentioned memory measure, and transmits.

A sending set which it has.

A reception means which receives the above-mentioned packet transmitted from the above-mentioned sending set, and a decode means which changes a decoder according to the above-mentioned packet, An extraction means to extract the above-mentioned sleep period from the above-mentioned packet, a memory measure which memorizes the above-mentioned sleep period, and a control means which stops receiving operation based on the above-mentioned sleep period, and shifts to sleeping.

[Claim 2]Before stopping a send action or receiving operation based on the above-mentioned sleep period by the above-mentioned control means of the above-mentioned sending set or the above-mentioned receiving set and shifting to sleeping, behind, The transmission and reception system according to claim 1 starting the above-mentioned send action or the above-mentioned receiving operation, and making it shift to the Wake state.

[Claim 3]The transmission and reception system according to claim 1 delaying time to stop a send action or receiving operation based on the above-mentioned sleep period by the above-mentioned control means of the above-mentioned sending set or the above-mentioned receiving set, and shift to sleeping according to the length of a packet transmitted or received.

[Claim 4]The transmission and reception system according to claim 1 shifting an electric power supply state about the above-mentioned send action or the above-mentioned receiving operation to low-power-consumption mode during the above-mentioned sleep, and/or reducing a clock frequency of the above-mentioned control means.

[Claim 5]The transmission and reception system according to claim 4 disconnecting current supply to the above-mentioned transmitting means or the above-mentioned reception means which is not used in the above-mentioned low-power-consumption mode.

[Claim 6]The transmission and reception system according to claim 4 shifting to the above-mentioned low-power-consumption mode during the above-mentioned sleep, and disconnecting current supply to the above-mentioned encode means or the above-mentioned decode means of the above-mentioned sending set or the above-mentioned receiving set.

[Claim 7]The transmission and reception system according to claim 1, wherein the above-mentioned sleep period setting-out means transmits the above-mentioned sleep period by the above-mentioned logical channel by setting up a user definition command using a logical channel different from the above-mentioned packet.

[Claim 8]The transmission and reception system according to claim 1 characterized by transmitting the above-mentioned sleep period using a header part or an user definition field of the above-mentioned packet.

[Claim 9]The transmission and reception system according to claim 4 characterized by controlling periodically power saving to the above-mentioned encode means or the above-mentioned decode means according to timing which acquires the

above-mentioned input signal or the above-mentioned packet of the above-mentioned sending set or the above-mentioned receiving set irrespective of the above-mentioned sleep period.

[Claim 10]The transmission and reception system according to claim 1 transmitting two or more frames collectively about the above-mentioned packet of the above-mentioned sending set.

[Claim 11]The transmission and reception system according to claim 1 setting up a maximum of setting out which does not resend, or a retry count, and setting up a periodic period which can shift to sleeping beforehand about the above-mentioned packet of the above-mentioned sending set.

[Claim 12]A transmitting and receiving method which it transmits to an input signal by performing sending-signal processing from a sending set characterized by comprising the following in a network, and performs and outputs a reception signal processing to a signal received in a receiving set in the above-mentioned network.

An encoding step which is processing in a sending set and changes an encoder according to the above-mentioned input signal.

A sleep period setting step which sets a sleep period which stops a send action according to an encode signal from the above-mentioned encoding step, and is made into sleeping to an enabled change.

A memory step which memorizes the above-mentioned sleep period.

A control step which stops a send action based on the above-mentioned sleep period, and shifts to sleeping.

A transmission step which inserts in a packet the above-mentioned sleep period memorized by the above-mentioned memory step, and transmits.

A receiving step which receives the above-mentioned packet which is processing in a receiving set and is transmitted from the above-mentioned sending set.

A decoding step which changes a decoder according to the above-mentioned packet, an extraction step which extracts the above-mentioned sleep period from the above-mentioned packet, a memory step which memorizes the above-mentioned sleep period, and a control step which stops receiving operation based on the above-mentioned sleep period, and shifts to sleeping.

[Claim 13]The transmitting and receiving method according to claim 12 shifting an electric power supply state about the above-mentioned send action or the above-mentioned receiving operation to low-power-consumption mode during the above-mentioned sleep, and/or reducing a clock frequency of the above-mentioned

control step.

[Claim 14]The transmitting and receiving method according to claim 12 shifting to the above-mentioned low-power-consumption mode during the above-mentioned sleep, and disconnecting current supply to the above-mentioned encoding step or the above-mentioned decoding step of the above-mentioned sending set or the above-mentioned receiving set.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]This invention relates to the digital-analog converter using the method and it which amend the nonlinear error of a digital-analog converter by little amendment data.

[0002]

[Description of the Prior Art]A digital-analog converter inputs a digital signal and outputs the analog signal corresponding to the digital signal. The setting-out code of an input digital signal and an example of correspondence of an output analog signal are shown in drawing 8.

[0003]In drawing 8, a horizontal axis expresses the setting-out code of an input digital signal, and a vertical axis expresses the pressure value of an output analog signal. 91 is an ideal line which is the input / output relation of an ideal digital-analog converter, and has become a straight line. 92 is the input / output relation in a actual digital-analog converter, and has become a curve. That is, it has shifted from the ideal line 91 and a

nonlinear error exists.

[0004]93 is a calibration point, sets up the digital signal corresponding to these points, and measures the output value at that time. Such several calibration points are provided, and he assumes the curve which connects these calibration points, and is trying for it to amend the nonlinear error of a digital-analog converter.

[0005]

[Problem(s) to be Solved by the Invention]However, there was following SUBJECT in the correcting method of such a nonlinear error of a digital-analog converter.

[0006]Proofreading must be performed for every set and it takes time. If the number of a calibration point is lessened, proofreading time can be shortened, but if a nonlinear error does not use a small digital-analog converter from the first, an error will become large near [middle] the point of a calibration point. When a small digital-analog converter had an expensive nonlinear error and especially conversion of a multi-channel was required, SUBJECT that cost will become high occurred.

[0007]If a nonlinear error uses a cheap large digital-analog converter, in order to make the error after proofreading small, a calibration point must be increased, and it must proofread to all the input digital values depending on the case. Therefore, SUBJECT that the compensation table which proofreading takes a long time to and keeps calibration data will become large also occurred.

[0008]Therefore, there is the issue which this invention tends to solve in providing the correcting method of the nonlinear error of the digital-analog converter which proofreading is possible for a short time, and can lessen amendment data, and the digital-analog converter using it.

[0009]

[Means for Solving the Problem]In order to solve such SUBJECT, among this inventions the invention according to claim 1, A nonlinear error which is the nonlinear error correction method of a digital-analog converter composition of dividing and inputting a digital signal into two or more stages 1 and 2, and each of two or more of said stages 1 and 2 has is amended for every stage, A nonlinear error of said digital-analog converter is amended. Little amendment data can amend a nonlinear error.

[0010]The invention according to claim 2 is made to perform amendment of a nonlinear error of each of said stages 1 and 2 in the invention according to claim 1 using a compensation table. It can amend easily.

[0011]In a digital-analog converter of composition of the invention according to claim 3 comprising two or more stages 1 and 2, dividing and inputting a digital signal into the stages 1 and 2 of these plurality, and changing a digital signal into an analog signal, A

nonlinear error of a digital-analog converter is amended by amending a nonlinear error which two or more stages 1 and 2 have for every stage. Little amendment data can amend a nonlinear error correctly.

[0012]Two or more stages 1 and 2 from which the invention according to claim 4 changes an inputted digital signal into an analog signal, It has two or more compensation tables 81 (82) corresponding to each of two or more of these stages 1 (2), Divide and input into this compensation table 81 (82) a digital signal changed into an analog signal, and input into the stage 1 (2) which corresponds an output of this compensation table 81 (82), and. Data which amends a nonlinear error of a stage corresponding to the compensation table 81 (82) is stored. A nonlinear error can be amended easily.

[0013]In the invention according to claim 3 or 4, the invention according to claim 5 the stages 1 and 2, It is characterized by being a stage of composition of changing an input digital signal into an analog signal by carrying out the partial pressure of the output analog signal of reference voltage or a preceding paragraph stage using a resister network. It is applicable to a general-purpose digital-analog converter.

[0014]

[Embodiment of the Invention]Below, based on figures, this invention is explained in detail. The composition of the digital-analog converter of a bit (n+k) is shown in drawing 1. This digital-analog converter has the composition that two stages, the 1st stage 1 and the 2nd stage 2, were connected in series. Top n-bit conversion is performed on the 1st stage 1, and a low rank k bit is changed on the 2nd stage 2.

[0015]The 1st stage 1 is a stage which performs rough conversion of an output analog signal, and the digital value of n bit is inputted. n resistance R1_ [with the resistance with that same internal configuration] (2^n-1) - R1_0 is connected in series, one end of this series circuit is connected to the high-level reference voltage side REFH, and the other end is connected to the low the reference voltage side REFL.

[0016]As the end of switch SW1_2^n-SW 1_0 of an individual shows drawing 1, it is connected to the node of resistance R1_ (2^n-1) - R1_0 and FERH of reference voltage, and each (n+1) of REFL in order. Every other 1, i.e., SW1_2^n, and SW1_2^n-2 from switch SW1_2^n, and SW1_2^n-4 .... The other end of the switch to the input terminal of buffer Buf1 with the other other end of SW1_0 is connected to the input terminal of buffer Buf2.

[0017]The 2nd stage 2 also has the same composition as the 1st stage 1. That is, the series connection of k resistance R2_ (2^k-1) - R2_0 is carried out, one end of this series circuit is connected to the output terminal of buffer Buf1, and the other end is connected to the output terminal of buffer Buf2. As shown in drawing 1 (k+1), one end of switch

SW2_2^k-SW 2_0 of an individual is connected to each of the output terminal of the node of these resistance and buffer Buf1, and Buf2, and the other end is connected to the input terminal of buffer Buf3. The output of buffer Buf3 turns into an output of a digital-analog converter.

[0018]Next, operation of this digital-analog converter is explained using drawing 2 and drawing 3. Drawing 2 is the figure with which the input digital value explained the operation at the time of 0 to (The k-th power of 2 - 1). Identical codes are given to the same element as drawing 1, and explanation is omitted.

[0019]In this case, the input digital value of the 1st stage 1 is set to 0. Switch SW1_1 of the 1st stage 1 and SW1_0 are made one, and other switches of the 1st stage 1 are turned OFF. The output of buffer Buf1 is set to REFL and the output of buffer Buf2 becomes (REFH-REFL)/(2 n-th power). Therefore, if the one [the switch of the 2nd stage 2] in the direction of the arrow 3 from SW2_2^k to SW2_0 in order, the output of buffer Buf3, i.e., the output of a digital-analog converter, increases from 0.

[0020]As for drawing 3, an input digital value shows the operation in (** (k+1)-1 of 2) from (the k-th power of 2). Identical codes are given to the same element as drawing 1, and explanation is omitted. In this case, the input digital value of the 1st stage 1 is set to 1. Only SW_1 and SW_2 are made one among the switches of the 1st stage 1, and other switches are turned OFF.

[0021]Since the output of buffer Buf1 becomes (REFL+(REFH-REFL)/(2 n-th power)) and the output of buffer Buf2 becomes (REFL+2x(REFH-REFL)/(2 n-th power)), If the one [the switch of the 2nd stage 2 / 0 / SW2_] in the direction of the arrow 4 in order, the output of buffer Buf3, i.e., the output of a digital-analog converter, increases.

[0022]That is, if the digital value inputted into the 1st stage 1 is set to p (n-th power of 0<=p<2 - one), switch SW1_p and SW1_p+1 will be turned on. If the switch of the 2nd stage 2 is made into turn from SW2_2^k at one at this time when the number of p is even, the output of a digital-analog converter will increase. If similarly turn is used from SW2_0 at one when the number of p is odd, the output of a digital-analog converter will increase.

[0023]The number of bits of the input digital value of a digital-analog converter Thus, m, The number of bits of the input digital value of the 1st stage 1 and the 2nd stage 2, respectively n, If k, it will become m=n+k, and top n bits inputted into the 1st stage 1 turn into top n bits of a digital-analog converter, and the low rank k bit inputted into the 2nd stage 2 turns into a low rank k bit of a digital-analog converter.

[0024]Next, the nonlinear error of this digital-analog converter is explained. Drawing 4 expresses a nonlinear error typically, a horizontal axis is an input digital value and a

vertical axis is an analog value of an output. 5 is an ideal line and expresses input-output behavioral characteristics in case there is no nonlinear error.

[0025]61-6q are the section 1 - the section q (n-th power of =2), and express the characteristic when the switch of the 2nd stage 2 is carried out to one at the turn shown in drawing 2 and drawing 3 in the time of input digital value p of the 1st stage being zero to q-1, respectively.They are the characteristic in case 611 does not have a nonlinear error of the 2nd stage 2 in the section 1 (p= 0), and the characteristic in case 612 has a nonlinear error. The characteristic in case there is no nonlinear error of the 2nd stage 2 similarly about the section 2 - the section q, and the characteristic at a certain time are shown.

[0026]Although the starting point and the terminal point of each section must be on the ideal line 5 ideally, it has shifted from the ideal line 5 for the nonlinear error of the 1st stage 1. The input digital value (= the number of the sections of drawing 4) of the 1st stage 1 is that of ****** (2 n-th power), and if the starting point and the terminal point of each section are taken into consideration, the amendment data of **** (n+1) of 2 can amend it.

[0027]Drawing 5 extracts and displays only the nonlinear error of the 2nd stage 2 of each section. Identical codes are given to the same element as drawing 4, and explanation is omitted. As drawing 2 and drawing 3 explained, since the turn [one / turn / the switch of the 2nd stage 2] becomes reverse, the even number section and the odd number section are symmetrical [the curve of a nonlinear error] in these sections.

[0028]Next, how to amend the nonlinear error of the 2nd stage 2 based on drawing 6 is explained. As mentioned above, the nonlinear error of the 2nd stage 2 will become the same curve by each class, if the two adjacent sections are made into one group. Therefore, the compensation table of one group is applicable to other groups of all the.

[0029]If a group is made in the sections 71 and 72 of drawing 6, the compensation table of this group is applicable also to other groups. By doing in this way, the nonlinear error which originates in the 2nd stage 2 on the table of **** (k+1) of 2 can be amended.

[0030]The composition of the digital-analog converter which has a compensation table which amends the nonlinear error which is one example of this invention is shown in drawing 7. Identical codes are given to the same element as drawing 1, and explanation is omitted.

[0031]In drawing 7, 81 is a compensation table which amends the nonlinear error of the 1st stage 1, and top n bits of an input digital value are inputted. This compensation table 81 outputs the digital value which amended the nonlinear error of the 1st stage 1 to the 1st stage 1. 82 is a table which amends the nonlinear error of the 2nd stage 2, and

the low rank k bit of an input digital value is inputted, and it outputs the amended digital value to the 2nd stage 2.

[0032]The correction value of **** (n+1) of 2 is stored in the compensation table 81, and the correction value of **** (k+1) of 2 is stored in the compensation table 82. However, if the starting point and a terminal point are taken into consideration, the size of a compensation table can be made into {** (k+1) of ** (n+1)+2 of 2 - 4} points on the whole.

[0033]Although this example explained the digital-analog converter which has two stages, it is also applicable to the digital-analog converter which has three or more stages.

[0034]Although the partial pressure of the output of the stage of reference voltage or the preceding paragraph was carried out and the digital-analog converter of composition of taking out the voltage which carried out the switch to one and carried out the partial pressure to turn was explained in this example, If it is a digital-analog converter which has two or more stages, it is applicable also to the digital-analog converter of composition of not using the resister network or resister network of other composition.

[0035]Not only the nonlinear error resulting from a resister network but the thing for which the nonlinear error resulting from other factors, for example, current cell, is amended is possible.

[0036]

[Effect of the Invention]According to this invention, the following effect is expectable clearly from having explained above. According to the invention according to claim 1, it is the nonlinear error correction method of the digital-analog converter composition of that a digital signal is divided and inputted into two or more stages 1 and 2, As the nonlinear error which each of two or more of said stages 1 and 2 has was amended individually, the nonlinear error of the digital-analog converter was amended.

[0037]A nonlinear error can be amended nearly thoroughly and the number of amendment data, i.e., a calibration point, can be reduced substantially. Therefore, it is effective in the ability to reduce substantially the time which can use the cheap large digital-analog converter of a nonlinear error, and proofreading takes.

[0038]According to the invention according to claim 2, in the invention according to claim 1, it was made to perform amendment of the nonlinear error of the stages 1 and 2 using the compensation table. It is effective in the ability to perform exact amendment with the easy composition in digital one only by preparing the compensation table in which amendment data was stored.

[0039]In the digital-analog converter of composition of according to the invention according to claim 3, comprising two or more stages 1 and 2, dividing and inputting a

digital signal into the stages 1 and 2 of these plurality, and changing a digital signal into an analog signal, The nonlinear error of the digital-analog converter was amended by amending the nonlinear error which two or more stages 1 and 2 have for every stage.

[0040]A nonlinear error can be amended nearly thoroughly and the number of amendment data, i.e., a calibration point, can be reduced substantially. Therefore, it is effective in the ability to reduce substantially the time which can use the cheap large digital-analog converter of a nonlinear error, and proofreading takes.

[0041]Two or more stages 1 and 2 which change the inputted digital signal into an analog signal according to the invention according to claim 4, It has two or more compensation tables 81 (82) corresponding to each of two or more of these stages 1 (2), Divide and input into this compensation table 81 (82) the digital signal changed into an analog signal, and input into the stage 1 (2) which corresponds the output of this compensation table 81 (82), and. The data which amends the nonlinear error of a stage was stored in the corresponding compensation table 81 (82).

[0042]A nonlinear error can be amended nearly thoroughly and the number of amendment data, i.e., a calibration point, can be reduced substantially. Therefore, it is effective in the ability to reduce substantially the time which can use the cheap large digital-analog converter of a nonlinear error, and proofreading takes. It is effective in the ability to amend simply and correctly only by preparing a compensation table.

[0043]For example, in the case of the 14-bit digital-analog converter which performs top 7 bits on the 1st stage, and performs low rank 7 bit conversion on the 2nd stage, when all points are amended, the calibration point of 16384 points and amendment data are needed, but. In this invention, the calibration point and amendment data of a 508-point (256+256-4) point can amend an equivalent nonlinear error.

[0044]In the invention according to claim 3 or 4, the invention according to claim 5 the stages 1 and 2, It was characterized by being a stage of composition of changing an input digital signal into an analog signal by carrying out the partial pressure of the output analog signal of reference voltage or a preceding paragraph stage by a resister network. It is effective in being applicable to the resister network type digital-analog converter used general-purpose.

[Translation done.]